PWDC008N04UESQ

Perfect MOS N-MOSFET 40V, 0.64mΩ, 348A

重庆平伟实业股份有限公司

Features

- Uses PingWei advanced PerfectMOS2 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g x R_{DS(on)}$ product(FOM)
- Qualified according to AEC-Q101 criteria

Benefits

- High robustness and reliability
- Increases maximum current capability
- Low power loss, high power density
- Easy paralleling

Applications

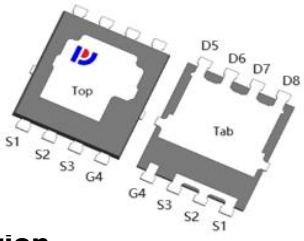
- General automotive applications
- EPS(Electric Power Steering)
- DC-DC

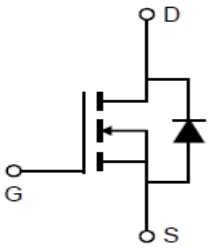
100% DVDS Tested
100% AvalancheTested

Product Summary

V_{DS}	40V
$R_{DS(on)@10V\ typ}$	0.64mΩ
$I_{D\ (Silicon\ limit)}$	348A

UPDFN5*6 Double Cooling





Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
PWDC008N04UESQ	PW0804U	UPDFN5*6 Double Cooling	Tape&Reel	13 inches	12mm	5000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	40	V
Continuous drain current T_C = 25°C (Silicon limit) T_C = 100°C (Silicon limit) T_C = 100°C (Package limit) Ta = 25°C (See RthJA)	I_D	 348 246 175 46	A
Pulsed drain current (T_C = 25°C)	$I_{D\ pulse}$	700	A
Avalanche energy, single pulse (L=0.1mH)	E_{AS}	435	mJ
Gate-Source voltage	V_{GS}	±20	V
Power dissipation T_C = 25°C Ta = 25°C (See RthJA)	P_{tot}	 171 3.0	W
Operating junction and storage temperature	T_j , T_{stg}	-55...+175	°C
Reflow soldering temperature（10s）	Tsold	260	°C

Thermal Resistance

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – case.	RthJC	-	0.75	0.9	°C/W	-
Thermal resistance , Channel to Top Plate	Rth(ch-tp)	-	-	0.95	°C/W	Note1
Thermal resistance, junction - ambient	RthJA	-	-	49.5	°C/W	Note2

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	**Symbol**	**Value**			**Unit**	**Test Condition**
		min.	**typ.**	**max.**		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	40	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	2.0	-	3.0	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 100	μA	V_{DS}=40V,V_{GS}=0V T_j=25°C T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.64	0.79	mΩ	Vgs=10V,Id=30A
Transconductance	g_{fs}	-	257	-	S	V_{DS}=5V,I_D=50A
Dynamic Characteristic						
Input Capacitance	C_{iss}	-	7282	-	pF	V_{GS}=0V, V_{DS}=20V, f=300KHz
Output Capacitance	C_{oss}	-	2318	-		
Reverse Transfer Capacitance	C_{rss}	-	55	-		
Gate Total Charge	Q_G	-	100	-	nC	Vds=20V,Id=30A ,Vgs=10V
Gate-Source charge	Q_{gs}	-	33	-		
Gate-Drain charge	Q_{gd}	-	12	-		
Turn-on delay time	$t_{d(on)}$	-	20	-	ns	V_{GS}=10V, V_{DD}=20V, R_{G_ext}=1.6Ω,I_D=20A
Rise time	t_r	-	23	-		
Turn-off delay time	$t_{d(off)}$	-	68	-		
Fall time	t_f	-	50	-		
Gate resistance	R_G	-	2.7	-	Ω	V_{GS}=0V, V_{DS}=0V, f=1MHz

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	-	1.2	V	V_{GS}=0V,I_{SD}=30A
Body Diode Continuous Forward Current	Is	-	-	175	A	TC = 25°C
Body Diode Pulsed Current	Is pulse	-	-	700	A	TC = 25°C
Body Diode Reverse Recovery Time	t_{rr}	-	130	-	ns	I_F=30A, dI/dt=100A/μs
Body Diode Reverse Recovery Charge	Q_{rr}	-	300	-	nC	

Note 1：A maximum of the Rth(ch-tp) measured at Pingwei's test environment is only used for reference.Beaware that the top-plate has the same electric potential as the sources; however,not intended for an Electrode.
Note 2:27mm x 20mm x 1.6mm FR-4、1oz、1 layer PCB,Top plate has no heatsink.

Typical Performance Characteristics

Fig 1: Output Characteristics

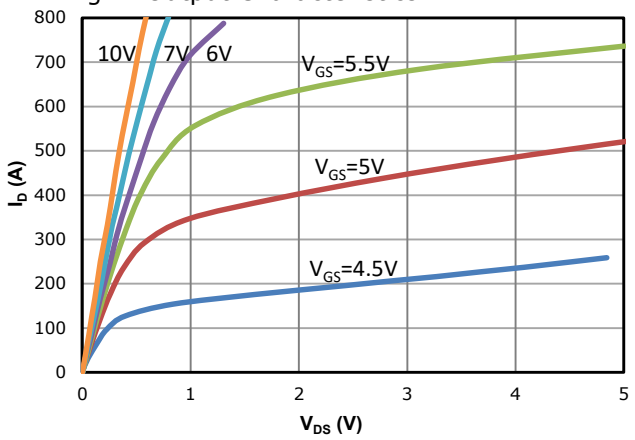


Fig 2: Transfer Characteristics

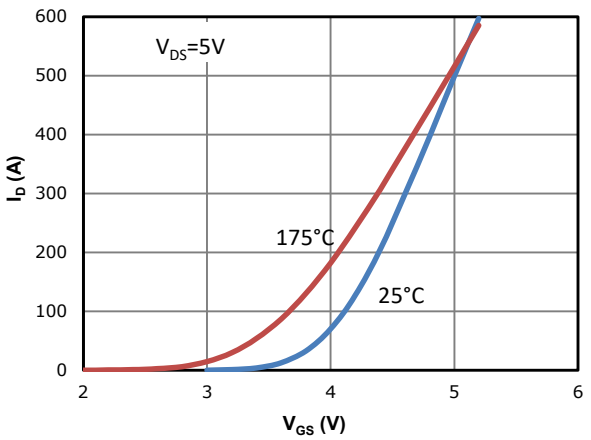


Fig 3: Rds(on) vs Drain Current and Gate Voltage

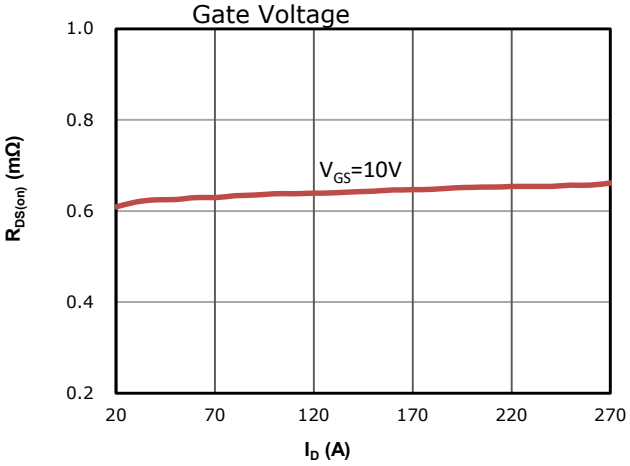


Fig 4: Rds(on) vs Gate Voltage

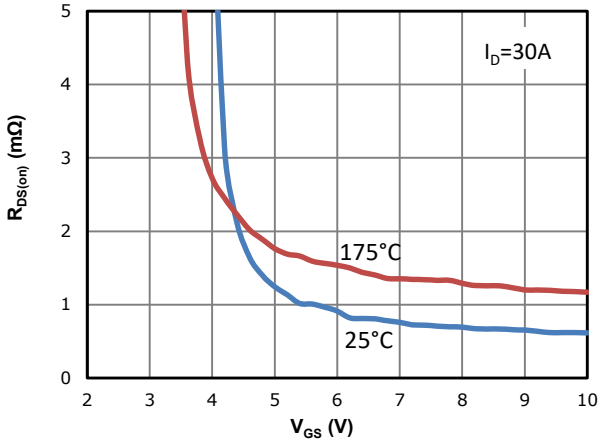


Fig 5: Rds(on) vs. Temperature

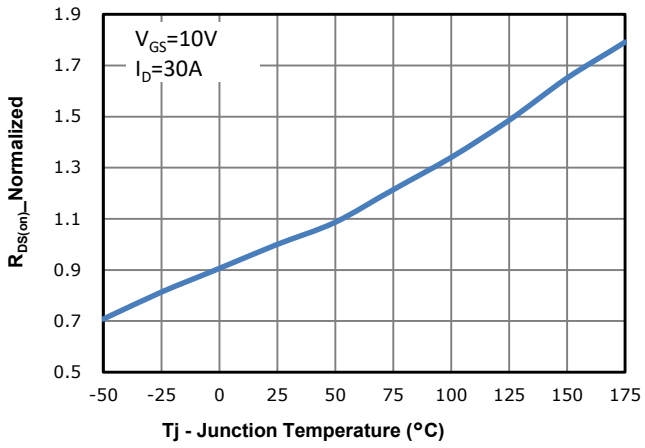


Fig 6: Vgs(th) vs. Temperature

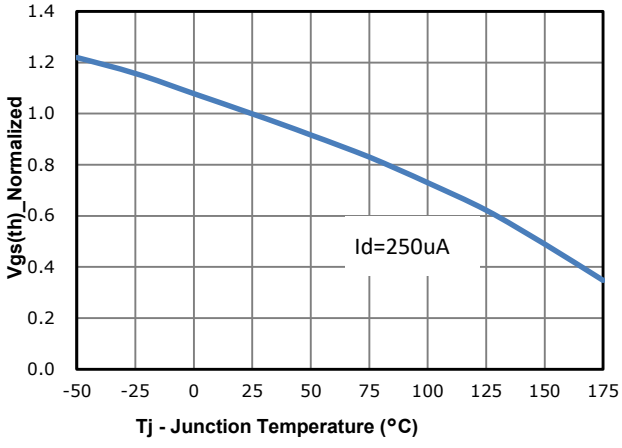


Fig 7: BVdss vs. Temperature

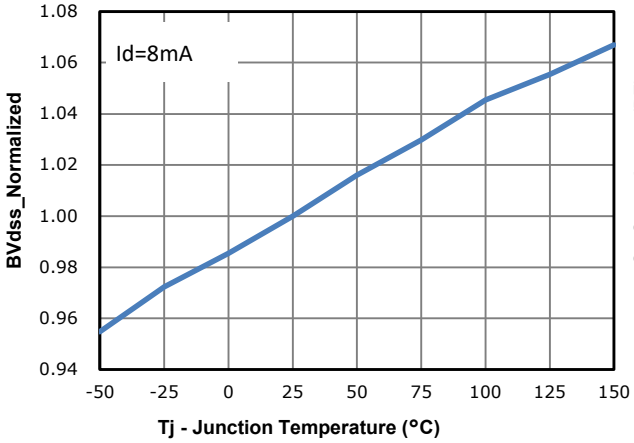


Fig 8: Capacitance Characteristics

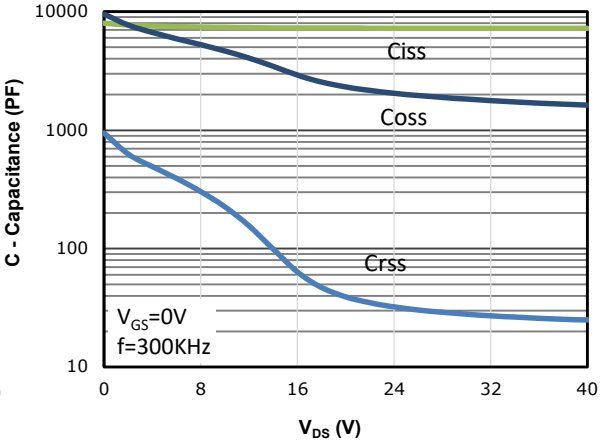


Fig 9: Gate ChargeCharacteristics

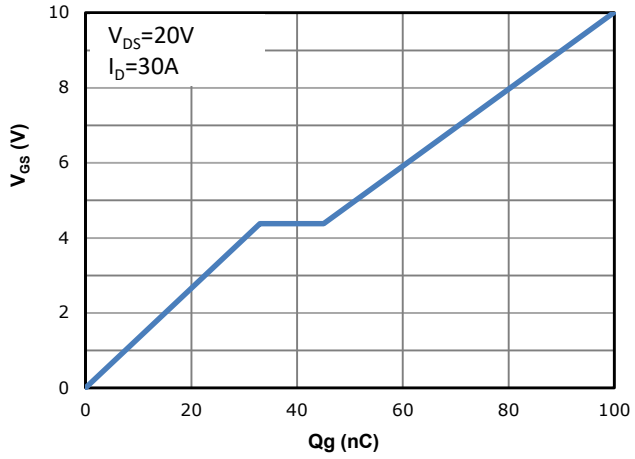


Fig 10: Body-diode Forward Characteristics

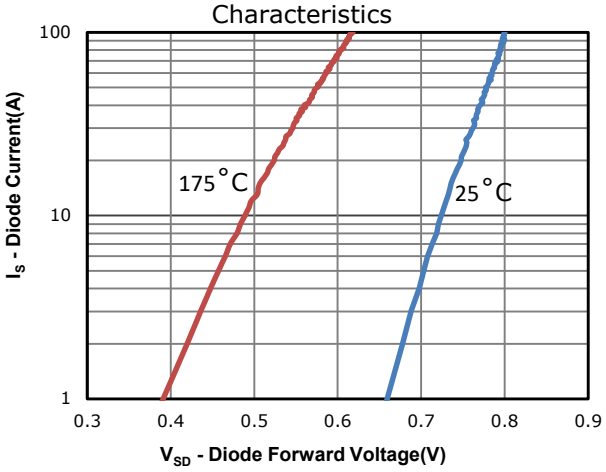


Fig 11: Power Dissipation

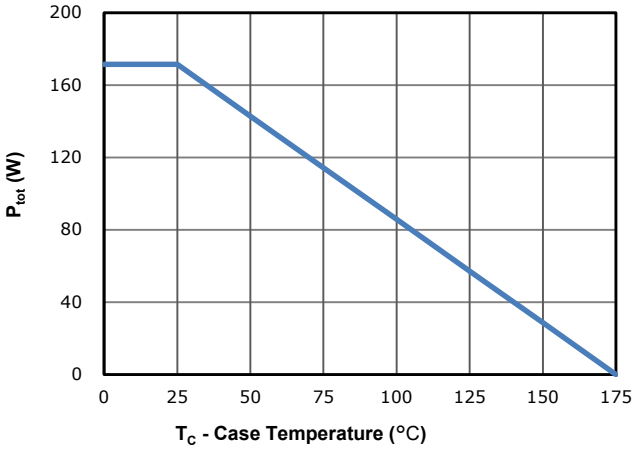


Fig 12: Drain Current Derating

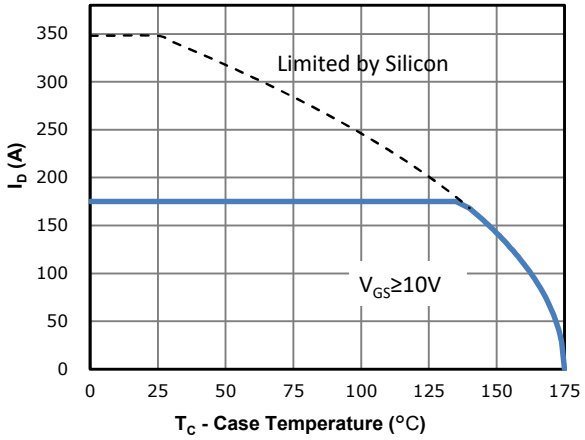


Fig 13: Safe Operating Area

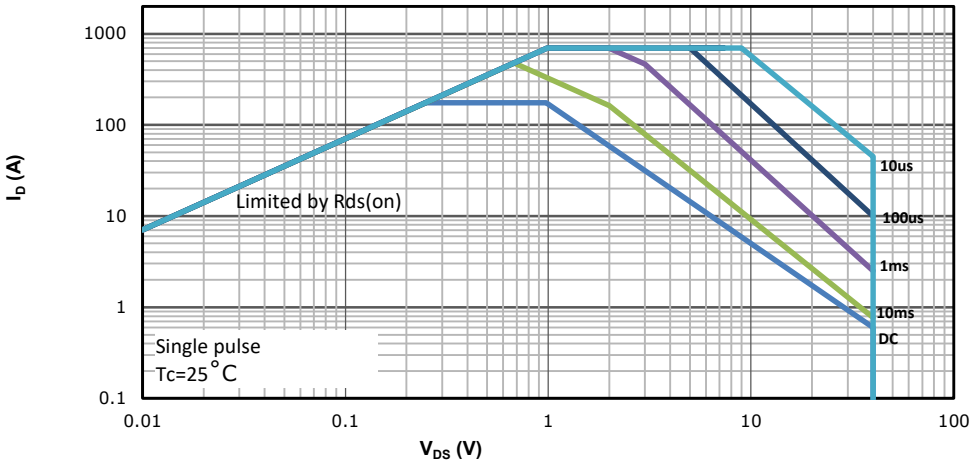
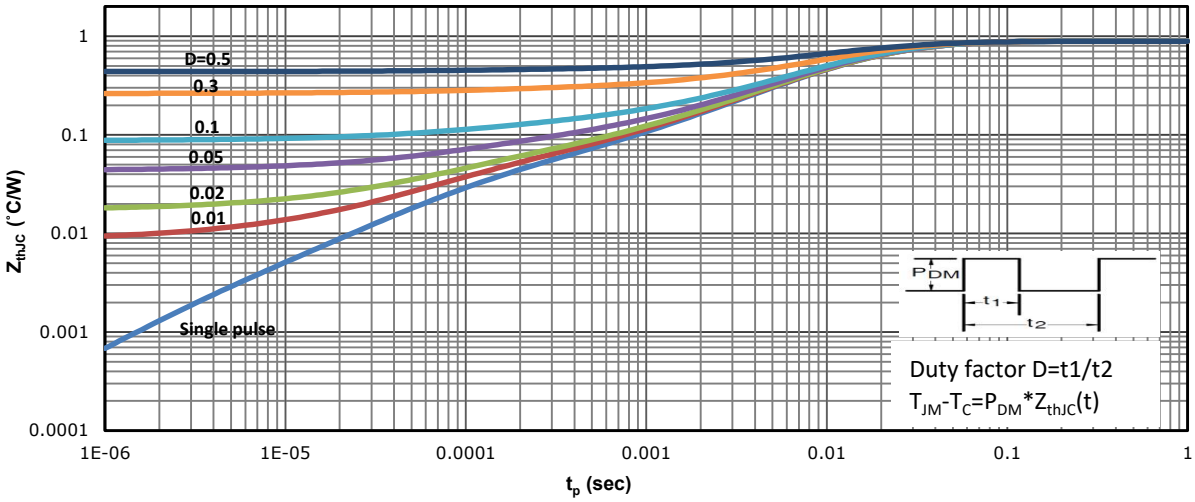
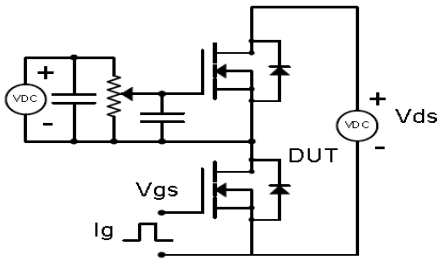


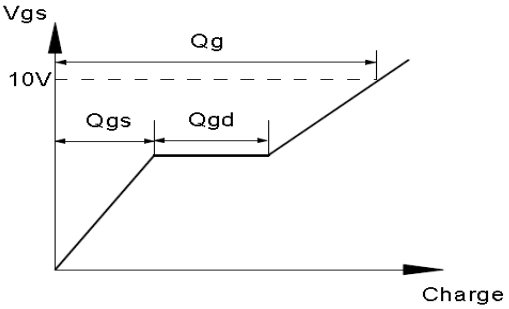
Fig 14: Max. Transient Thermal Impedance



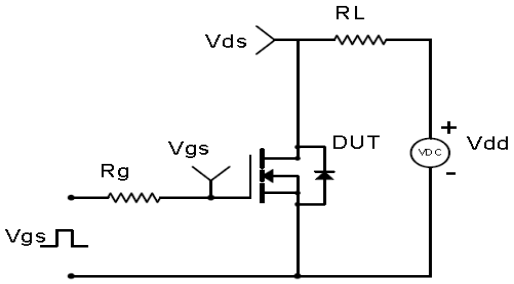
Test Circuit & Waveform

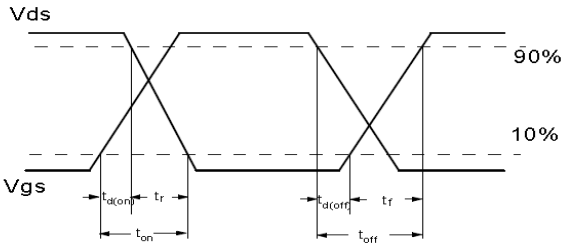
Gate Charge Test Circuit & Waveform



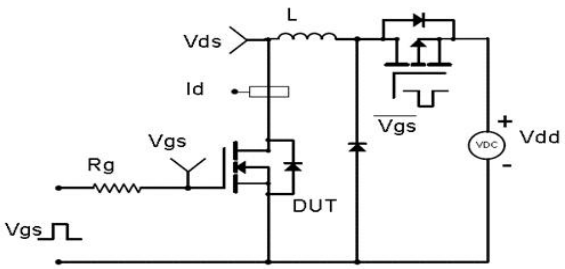


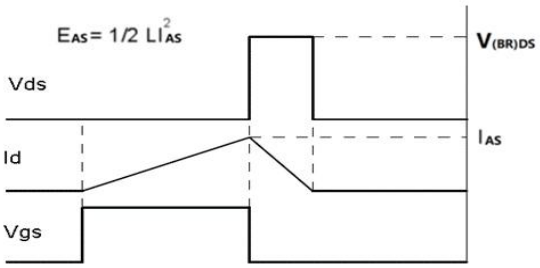
Resistive Switching Test Circuit & Waveforms



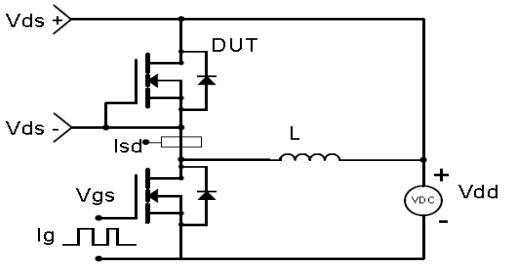


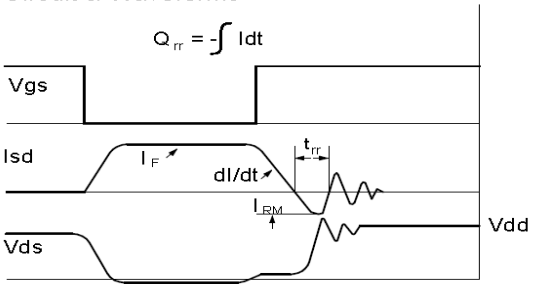
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



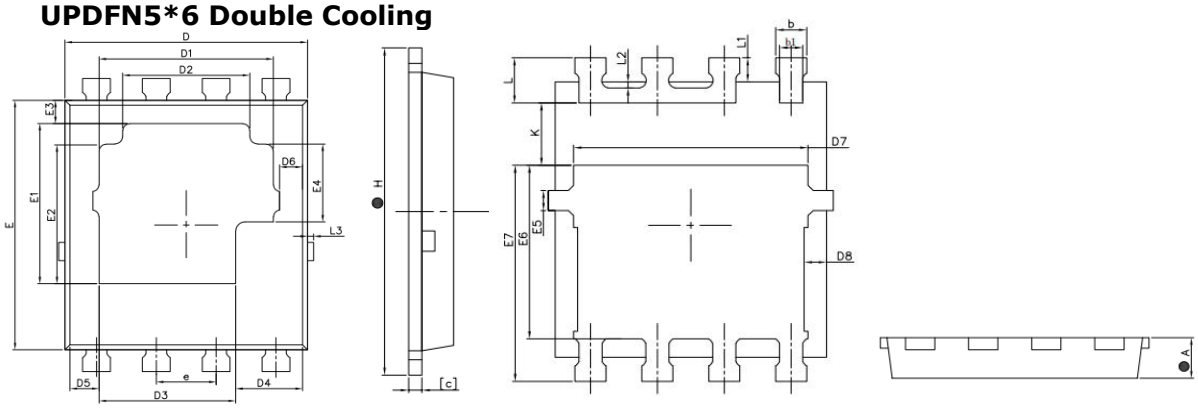


Diode Recovery Test Circuit & Waveforms





UPDFN5*6 Double Cooling



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.75	0.95	0.030	0.037
b	0.49	0.69	0.019	0.027
b1	0.34	0.54	0.013	0.021
c	0.20	0.30	0.008	0.012
D	4.95	5.35	0.195	0.211
D1	3.45	3.95	0.136	0.156
D2	2.45	2.95	0.096	0.116
D3	2.65	3.15	0.104	0.124
D4	1.17	1.67	0.046	0.066
D5	0.37	0.87	0.015	0.034
D6	0.29	0.69	0.011	0.027
D7	4.45	4.85	0.175	0.191
D8	0.23	0.63	0.009	0.025
E	5.28	5.68	0.208	0.224
E1	3.27	3.77	0.129	0.148
E2	2.80	3.30	0.110	0.130
E3	0.50	1.10	0.020	0.043
E4	1.46	1.96	0.057	0.077
E5	0.25	0.60	0.010	0.024
E6	3.20	3.70	0.126	0.146
E7	4.05	4.55	0.159	0.179
e	1.27		0.050	
H	6.19	6.69	0.244	0.263
L	0.65	1.15	0.026	0.045
L1	0.28	0.68	0.011	0.027
L2	0.12		0.005	
L3	-	0.23	-	0.009
K	1.04	1.44	0.041	0.057

Revision History

Revison	Date	Major changes
1.0	2024/10/15	Release of Formal Version.
1.1	2024/12/6	Update pakage ID limit from 150A to 175A;
1.2	2025/1/7	Update Outline D7 from 4.25-4.65 to 4.45-4.85,E3 from 0.26-0.76 to 0.5-1.1;
1.3	2025/3/17	Update Rjc & Zth & SOA;

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